

Fig. 1a

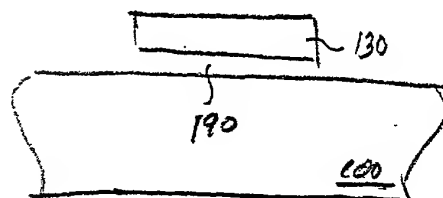


Fig. 1b

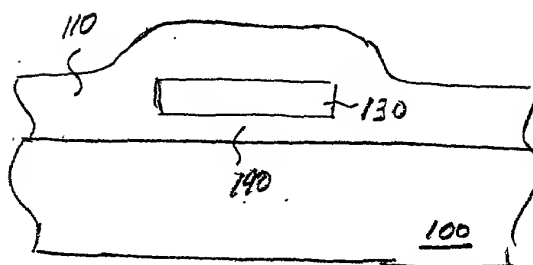


Fig. 1c

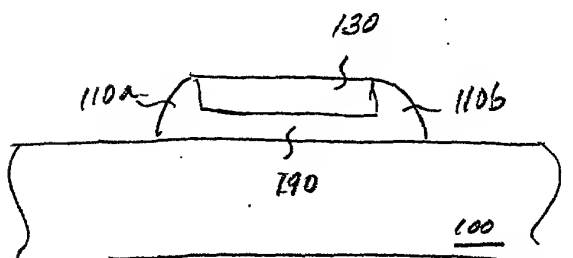


Fig. 1d

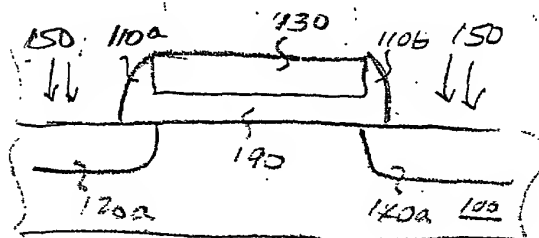


Fig. 1e

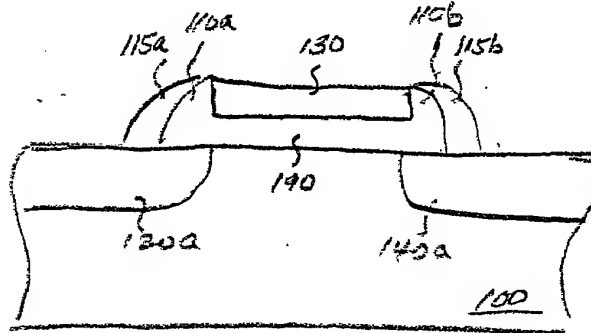


Fig. 1f

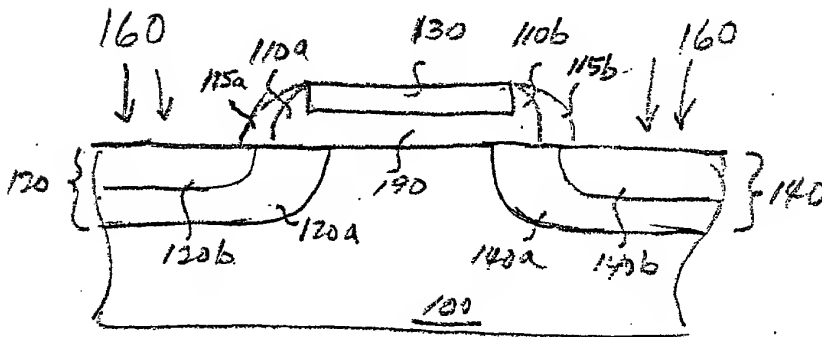


Fig. 1g

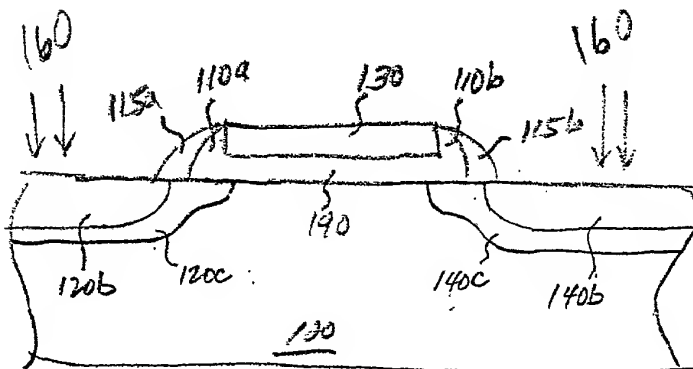


Fig. 2b

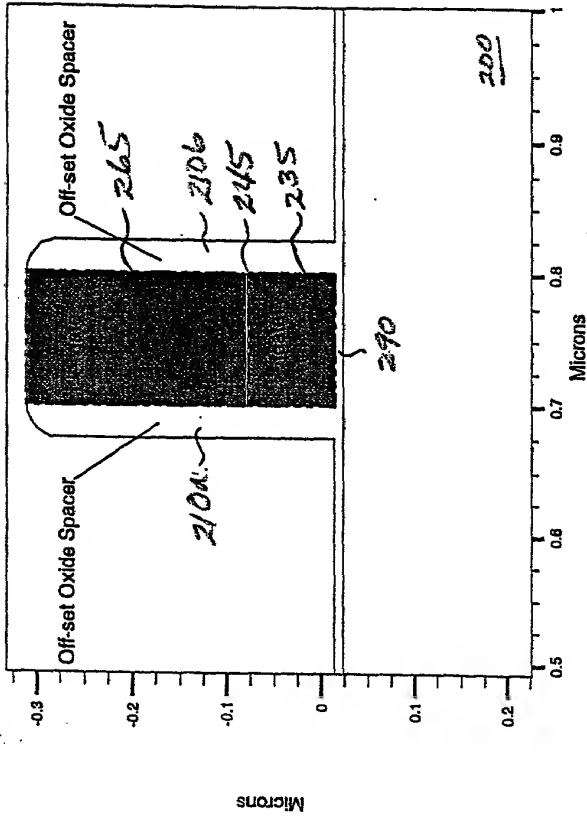


Fig. 2a

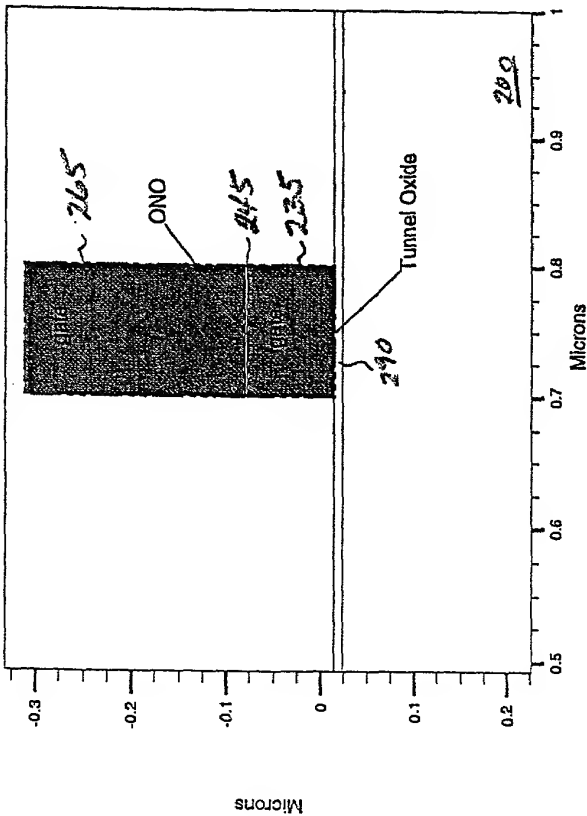


Fig. 2d

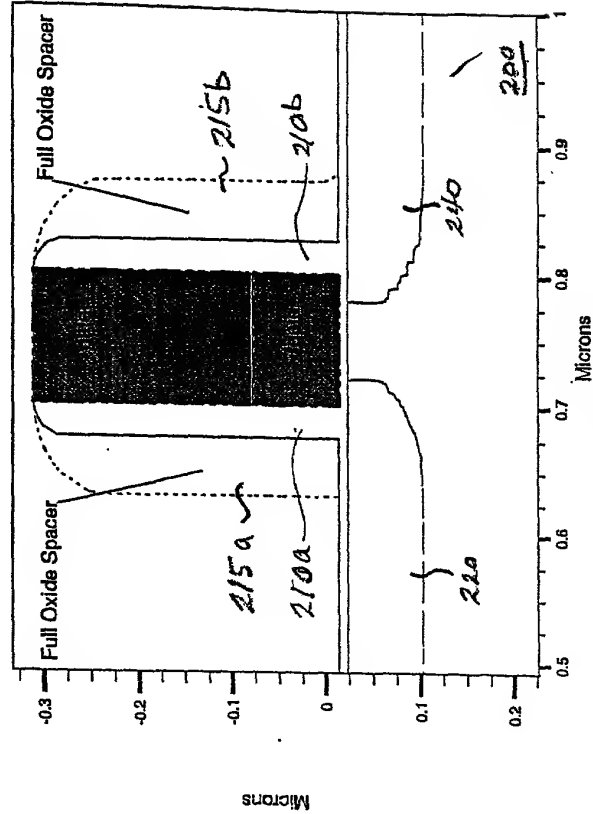
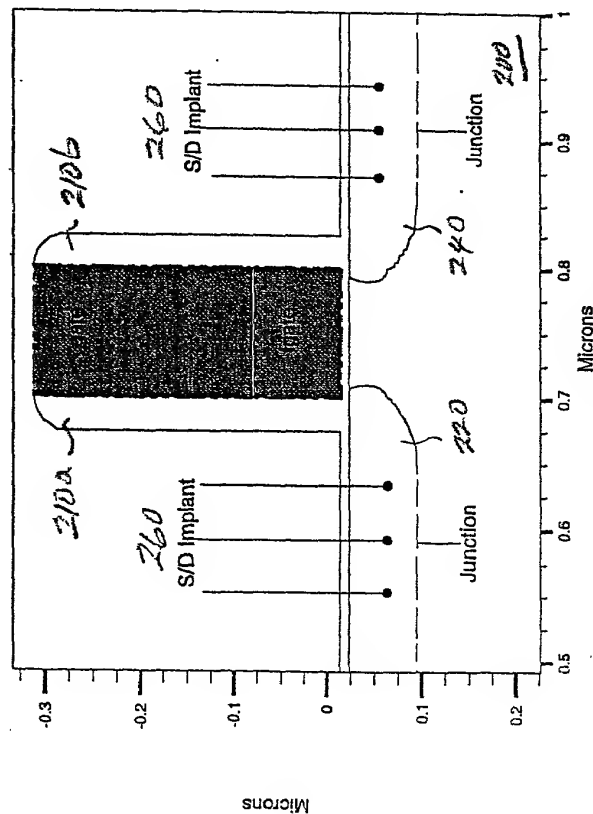


Fig. 2c



Array Cell

Fig. 3a



Fig. 3b



Fig. 3c

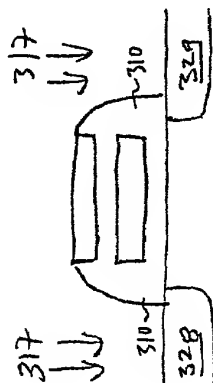
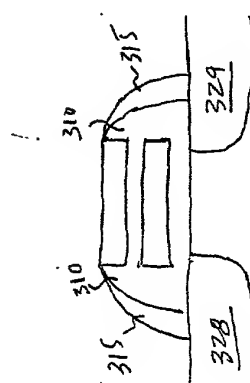
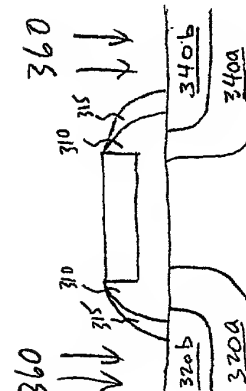
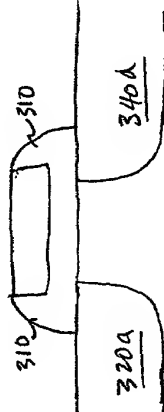
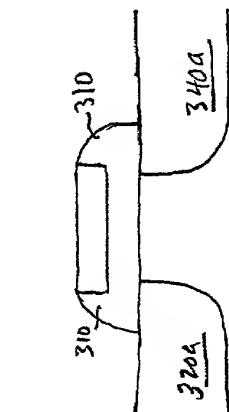
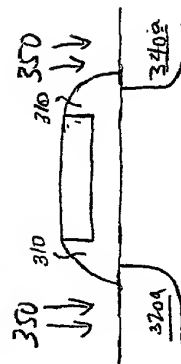


Fig. 3d



Peripheral DDD  
4V Transistor



Peripheral LDD  
LV Transistor

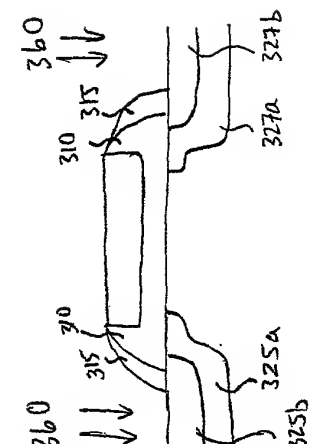
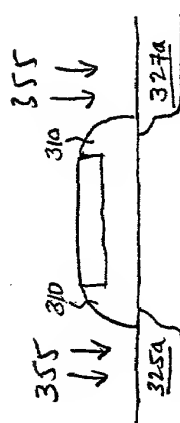
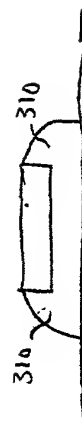


Fig. 4a

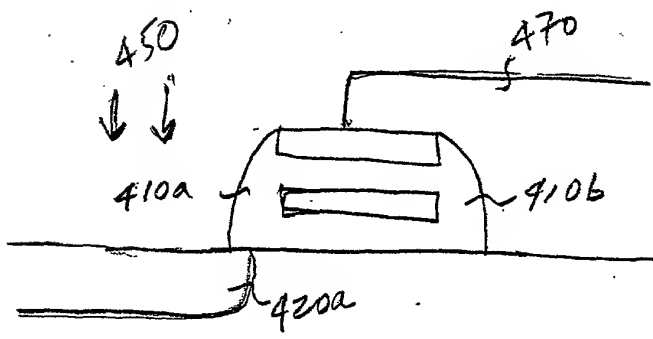


Fig. 4b

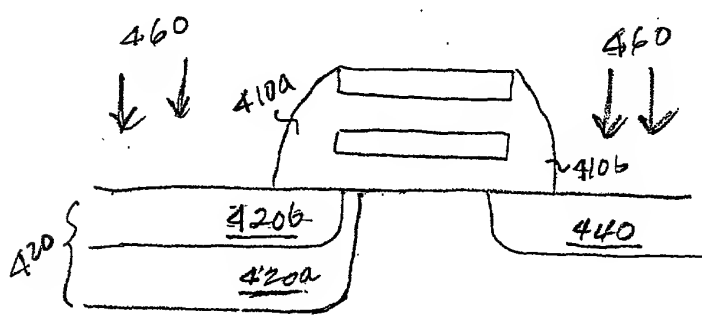


Fig. 5a

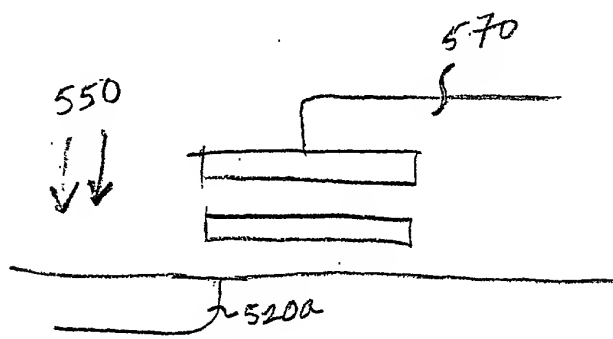


Fig. 5b

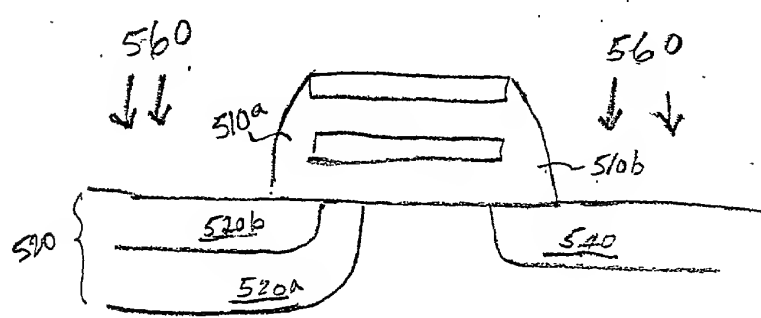


Fig. 6

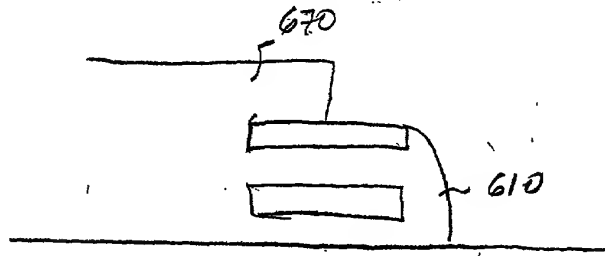


Fig. 7

